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Application Number

10/695,623

Filing Date

10/25/2003

First Named Inventor

Guy Even

Art Unit

Examiner Name

Attorney Docket Number

[illegible][illegible]

**Examiner
Signature**

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

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Application Number	10/695,623
Filing Date	10/25/2003
First Named Inventor	Guy Even
Art Unit	
Examiner Name	
Attorney Docket Number	

Sheet

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of

4

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	[1]	R.C. Agarwal, F.G. Gustavson, and M.S. Schmookler Series approximation methods for divide and square root in the power3 processor. In <i>Proceedings of the 14th IEEE Symposium on Computer Arithmetic</i> , volume 14, pages 116-123. IEEE, 1999	
	[2]	S. F. Anderson, J. G. Earle, R. E. Goldschmidt, and D. M. Powers. The IBM 360/370 model 91: floating-point execution unit. <i>IBM Journal of Research and Development</i> , January 1967	
	[5]	Marius A. Cornea-Hasegan, Roger A. Golliver, and Peter Markstein. Correctness proofs outline for Newton-Raphson based floating-point divide and square root algorithms. In <i>Proceedings of the 14th IEEE Symposium on Computer Arithmetic</i> , pages 96-105, April 1999. IEEE Computer Society Press	
	[6]	D. DasSarma and D. W. Matula. Faithful bipartite ROM reciprocal tables. In S. Knowles and W. H. McAllister, editors, <i>Proc. 12th IEEE Symposium on Computer Arithmetic</i> , pages 17-28, 1995	
	[7]	M. Daumas and D.W. Matula. Recorders for partial compression and rounding. Technical Report 97-01, Laboratoire de l'Informatique du Parallélisme, Lyon, France, 1997	
	[8]	M. Daumas and D.W. Matula. A Booth multiplier accepting both a redundant or a non-redundant input with no additional delay. In <i>IEEE International Conference on Application-specific Systems, Architectures and Processors</i> , pages 205-214, 2000	
	[9]	G. Even, S.M. Mueller, and P.M. Seidel. A Dual Mode IEEE multiplier. In <i>Proceedings of the 2nd IEEE International Conference on Innovative Systems in Silicon</i> , pages 282-289. IEEE, 1997	
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	[11]	G. Even and P.-M. Seidel. A comparison of three rounding algorithms for IEEE floating-point multiplication. <i>IEEE Transactions on Computers, Special Issue on Computer Arithmetic</i> , pages 638-650, July 2000	
	[12]	Guy Even and Peter-M. Seidel. Pipelined multiplicative division with IEEE rounding. In <i>Proceedings of the 21st International Conference on Computer Design</i> , October 13-15 2003	

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	[13]	Guy Even, Peter-M. Seidel, and Warren E. Ferguson. A parametric error analysis of Gold-schmidt's division algorithm. In <i>Proceedings of the 16th IEEE Symposium on Computer Arithmetic</i> , June 15-18 2003. Full version submitted to JCSS	
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	[24]	P. Montuschi and T. Lang. Boosting very-high radix division with prescaling and selection by rounding. <i>IEEE Transactions on Computers</i> , 50(1):13-27, 2001	
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	[34]	E.M. Schwarz. Rounding for quadratically converging algorithms for division and square root. In <i>Proceedings of the 29th Asilomar Conference on Signals, Systems and Computers</i> , volume 29, pages 600-603. IEEE, 1996	
	[35]	P.-M. Seidel. High-speed redundant reciprocal approximation. <i>INTEGRATION, the VLSI Journal</i> , 28:1-12, 1999	

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Sheet	4	of	4		

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